What is claimed is:

1. A semiconductor device comprising:

a first interlayer insulating layer;

a trench formed in the first interlayer insulating layer;

a conductive layer buried in the trench, the conductive layer having a surface thereof higher than a surface of the first interlayer insulating layer;

an insulating film having a flat surface and covering the first interlayer insulating layer and the conductive layer; and

a second interlayer insulating layer formed on the insulating film, the second interlayer insulating layer having a high etching selective ratio to the insulating film.

2. The semiconductor device according to claim 1, wherein a film thickness of the insulating film on the first interlayer insulating layer is greater than that on the conductive layer.

3. The semiconductor device according to claim 1, wherein the insulating film is made of a coating type material.

4. The semiconductor device according to claim 1, wherein the insulating film has an effect of preventing diffusion of a conductor material in the conductive layer.

5. The semiconductor device according to claim 1, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of an insulating material having a relative dielectric constant lower than that of an SiO_2 film.

6. The semiconductor device according to claim 1, wherein the insulating film is made of an insulating material having a relative dielectric constant lower than that of an SiO_2 film.

7. The semiconductor device according to claim 1, wherein the conductive layer includes a barrier metal layer.

8. The semiconductor device according to claim 1, wherein the conductive layer includes a Cu wiring layer.

9. The semiconductor device according to claim 1, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of methylpolysiloxane.

10. The semiconductor device according to claim 1, wherein the insulating layer is made of any one of polyarylene and benzo cyclo-butene.

11. A method of manufacturing a semiconductor device, comprising:

forming a first interlayer insulating layer;

forming a trench in the first interlayer insulating layer;

forming a conductive layer on the first interlayer insulating layer and burying the conductive layer in the trench simultaneously;

polishing a surface of a resultant structure after the formation of the conductive layer and forming a flat surface, to which the first interlayer insulating layer and the conductive layer are exposed;

etching a mechanically damaged layer due to the polishing, the mechanically damaged layer remaining on a surface of the first interlayer insulating layer;

forming an insulating film having a flat surface on the surface of the resultant structure after the etching; and

forming a second interlayer insulating layer, having a high etching selective ratio to the insulating film, on the insulating film.

12. The method according to claim 11, wherein the insulating film is formed by use of a coating method.

13. The method according to claim 11, further comprising:

partially etching the second interlayer insulating layer and the insulating film to form a contact hole having a bottom portion, to which at least a part of the conductive layer is exposed.

14. The method according to claim 11, wherein the insulating film is made of a material having an effect of preventing diffusion of a conductor material in the

conductive layer.

15. The method according to claim 11, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of a material having a relative dielectric constant lower than that of an SiO_2 film.

16. The method according to claim 11, wherein the insulating film is made of a material having a relative dielectric constant lower than at least that of an SiO_2 film.

17. The method according to claim 11, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of methylpolysiloxane.

18. The method according to claim 11, wherein the conductive layer includes a barrier metal layer.

19. The method according to claim 11, wherein the conductive layer includes a Cu wiring layer.

20. The method according to claim 11, wherein the etching, the formation of the insulating layer, and the formation of the second interlayer insulating layer are carried out under atmospheric pressure.

21. A method of manufacturing a semiconductor device, comprising:

forming a first interlayer insulating layer;

covering a surface of the first interlayer insulating layer with a protective film;

forming a trench in the first interlayer insulating layer covered with the protective film;

forming a conductive layer on a surface of a resultant structure after the formation of the trench and burying the conductive layer in the trench;

polishing the surface of the resultant structure after the formation of the conductive layer and forming a flat surface, to which the protective film and the conductive layer are exposed;

etching the protective film;

forming an insulating film having a flat surface on the resultant structure after the etching the protective film; and

forming a second interlayer insulating layer, having a high etching selective ratio to the insulating film, on the insulating film.

22. The method according to claim 21, wherein the insulating film is formed by use of a coating method.

23. The method according to claim 21, wherein the protective film is an SiO_2 film.

24. The method according to claim 21, wherein the insulating film has an effect of preventing diffusion of a conductor material in the conductive layer.

25. The method according to claim 21, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of a material having a relative dielectric constant lower than that of an SiO_2 film.

26. The method according to claim 21, wherein the insulating film has a relative dielectric constant lower than at least that of an SiO_2 film.

27. The method according to claim 21, wherein at least any one of the first interlayer insulating layer and the second interlayer insulating layer is made of methylpolysiloxane.

28. The method according to claim 21, wherein the conductive layer includes a barrier metal layer.

29. The method according to claim 21, wherein the conductive layer includes a Cu wiring layer.

30. The method according to claim 21, wherein the etching, the formation of the insulating layer, and the formation of the second interlayer insulating layer are carried out under atmospheric pressure.